REMARKS

Restriction Requirement

As indicated via telephone on June 18, 2004, in response to the restriction requirement, Applicant wishes to elect claims 1-18 and 27-32, set forth as species I by the examiner, without traverse. Therefore, applicant requests that claims 19-26 and 33-38 be withdrawn.

§ 102(b)

The Patent Office rejected claims 1, 2, 6, 10, 11, 14, 15, 17, 18, 27-29, and 32 under 35 U.S.C. § 102(b) as being anticipated by Graziadei (U.S. Patent No. 4,480,337). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 UPPQ 2d 1051, 1053 (Fed. Cir. 1987).*

Regarding claim 1, Graziadei fails to expressly or inherently disclose at least a mixer circuit comprising a gain stage coupled to receive a modulated bias current on a common node, the gain stage having a first current, a current shunt circuit coupled between the common node and a reference voltage, the current shunt circuit having a second current, wherein the first current and the second current are coupled to the common node, and a bias circuit to generate the modulated bias current.

Referring to Figure 2, Graziadei discloses a mixer and amplifier circuit including a first differential amplifier (T1-T4), a mixer differential amplifier (T5, T6), a current generator (T7), a double balanced mixer (T8-T11), and shunt transistors (T12, T13). As disclosed in col. 3, lines 46-57:

> When the average level of the input signal is high enough ..., the transistors T12 and T13 begin to conduct, effectively connecting (i.e. shunting) the input and the output of the circuit formed by the connection of the first input differential amplifier to the differential amplifier of the mixer. The shunt effect increases as the level of the signal increases, while the gain of the differential amplifiers decreases until these are completely inactive and the signal is introduced in the mixer circuit by only the transistors T12 and T13.

To ensure linear operation when the level of the RF input signal increases above a threshold, the shunt transistor (T12) shunts a common node of the transistors (T8, T9) of the double balanced mixer to the RF signal, and the shunt transistor (T13) shunts a common node of the transistors

(T10, T11) of the double balanced mixer to the RF signal. The shunt transistors (T12, T13) operate to shunt the RF signal to the input of the double balanced mixer (T8-T11) rather than to shunt current from a common node of a gain stage to a reference voltage. In other words, each of the shunt transistors (T12, T13) of Graziadei couple a common node of the double balanced mixer (T8-T11) to the RF signal rather than to a reference voltage. Since Graziadei fails to disclose a current shunt circuit coupled between a common node of a gain stage and a reference voltage, claim 1 is allowable.

For at least the same reason claim 1 is allowable, claims 2, 3, 5-18, and 27-32 are allowable. However, Applicant reserves the right to address the rejections of claims 2, 3, 5-18, and 27-32 in the future if necessary.

In view of the discussion above, claims 1-3, 5-18, and 27-32 are allowable. Reconsideration is respectfully requested. If any issues remain, the examiner is encouraged to contact the undersigned attorney of record to expedite allowance and issue.

Respectfully submitted,
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